ENHANCEMENT MODE GALLIUM NITRIDE POWER DEVICES

BACKGROUND

[0001] This disclosure is related to gallium nitride based semiconductor transistors.

[0002] Gallium nitride (GaN) semiconductor devices, which are III-V or III-nitride type devices, are emerging as an attractive candidate for power semiconductor devices because the GaN devices are capable of carrying large currents and supporting high voltages. Such devices are also able to provide very low on-resistance and fast switching times. A high electron mobility transistor (HEMT) is one type power semiconductor device that can be fabricated based on GaN materials. As used herein, GaN materials that are suitable for transistors can include secondary, tertiary, or quaternary materials, which are based on varying the amounts of the III type material of AlInGaN, Al, In and Ga, from 0 to 1, or $Al_xIn_yGa_{1-x-y}N$. Further, GaN materials can include various polarities of GaN, such as Ga-polar, N-polar, semi-polar or non-polar. In particular, N-face material may be obtained from N-polar or semi-polar GaN.

[0003] A GaN HEMT device can include a III-nitride semiconductor body with at least two III-nitride layers formed thereon. Different materials formed on the body or on a buffer layer causes the layers to have different band gaps. The different materials in the adjacent III-nitride layers also causes polarization, which contributes to a conductive two dimensional electron gas (2DEG) region near the junction of the two layers, specifically in the layer with the narrower band gap. One of the layers through which current is conducted is the channel layer. Herein, the narrower band gap layer in which the current carrying channel, or the 2DEG is located is referred to as the channel layer. The device also includes a gate electrode, a schottky contact and an ohmic source and drain electrodes on either side of the gate. The region between the gate and drain and the gate and source, which allows for current to be conducted through the device, is the access region.

[0004] The III-nitride layers that cause polarization typically include a barrier layer of AlGaN adjacent to a layer of GaN to induce the 2DEG, which allows charge to flow through the device. This barrier layer may be doped or undoped. In some cases, doping of the barrier layer may add to channel charge and it may also help in dispersion control. Because of the 2DEG typically existing under the gate at zero gate bias, most III-nitride devices are normally on or depletion mode devices. If the 2DEG is depleted, i.e., removed, below the gate at zero applied gate bias, the device can be an enhancement mode or normally off device.

[0005] Enhancement mode or normally off III-nitride type devices are desirable for power devices, because of the added safety they provide. An enhancement mode device requires a positive bias applied at the gate in order to conduct current. Although methods of forming III-nitride enhancement type devices are known, improved methods of depleting the 2DEG from under the gate in the channel layer are desirable.

SUMMARY

[0006] Devices are described that are enhancement mode devices with low off state leakage current as well as low on resistance. This is achieved in structures that result in not only depleting the 2DEG from under the gate region, but also have a high barrier to current flow under the gate region in the off state while ensuring that the region outside the gate, i.e., the access region, remains highly conductive.

[0007] In one aspect, a method of forming an N-face enhancement mode high electron mobility transistor device is described. The method includes forming on a substrate a Ga-faced sacrificial layer, forming a cap layer on the sacrificial layer, forming a GaN channel layer on the cap layer, forming an Al_xGaN layer on the channel layer, wherein $0 \leqq x \leqq 1$, forming a buffer layer on the Al_xGaN layer, bonding a carrier wafer on the buffer layer to form a stack, removing the substrate and the sacrificial layer from the stack to form an N-faced assembly of layers and forming a gate, source and drain on the N-faced assembly of layers.

[0008] In another aspect, a normally off III-nitride HEMT device is described. The device includes a gate, a source and a drain and an access region formed of a III-nitride material between either the source and the gate or the drain and the gate. In the access region the sheet resistance is less than 750 ohms/square. The device has an internal barrier under the gate of at least 0.5 eV, such as at least 1 eV, when no voltage is applied to the gate. The device is capable of supporting a 2DEG charge density under the gate of greater than $1\times10^{12}/cm^2$ in the on state.

[0009] In yet another aspect, a Ga-face enhancement mode high electrode mobility transistor device is described. The device includes a GaN buffer layer, a p-type bottom cap on the GaN buffer layer, wherein the GaN buffer layer has an aperture exposing the bottom cap, a GaN channel layer on an opposite side of the bottom cap from the GaN buffer layer, an Al_xGaN layer on an opposite side of the GaN channel layer from the cap layer, a p-type top cap on an opposite side of the Al_xGaN layer from the channel layer and a gate adjacent to the top cap.

[0010] In yet another aspect, a method of making a Ga-face enhancement mode high electrode mobility transistor device is described. The method includes forming a structure including the GaN buffer, GaN channel layer and Al_xGaN layer, forming the p-type top cap on the Al_xGaN layer, forming the gate adjacent to the p-type top cap, applying a passivation layer over the p-type top cap and Al_xGaN layer, bonding a carrier wafer onto the passivation layer and forming the aperture in the GaN buffer layer.

[0011] In another aspect, a Ga-face enhancement mode high electrode mobility transistor device is described. The device has a GaN buffer layer, an Al_xGaN layer on the GaN buffer layer, wherein the GaN buffer layer has an aperture exposing the Al_xGaN layer, a GaN channel layer on an opposite side of the Al_xGaN layer from the GaN buffer layer, an Al_yGaN layer on an opposite side of the GaN channel layer from the Al_xGaN layer, wherein a gate region of the Al_yGaN layer is treated with fluorine and an upper gate adjacent to the gate region. The fluorine treatment can include a treatment with a fluorine containing plasma.

[0012] In yet another aspect, a method of forming a Ga-face enhancement mode high electrode mobility transistor device is described. The method includes forming a structure of the GaN buffer layer, the Al_xGaN layer on the GaN buffer layer, wherein the GaN buffer layer has an aperture exposing a portion of the Al_xGaN layer, a GaN channel layer on an opposite side of the Al_xGaN layer from the GaN buffer layer and an Al_yGaN layer on an opposite side of the GaN channel layer from the Al_xGaN layer, treating the exposed portion of